CX1-BAND

CompactPCI® Intelligent Dual CAN2.0B Fieldbus Controller

User's Manual

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Contents

Contents . . . . . - 2 -

Figures . . . . . - 3 -

Tables . . . . . - 3 -

About this Manual . . . . . - 5 -
Edition History . . . . . - 5 -
Nomenclature . . . . . - 5 -
Trade Marks . . . . . - 5 -
Legal Exclaimer - Liability Exclusion . . . . . - 5 -

Introduction and Overview . . . . . - 6 -

Block Diagram . . . . . - 7 -

Handling Information . . . . . - 8 -
Precautions . . . . . - 8 -
Guidelines to EMC Protection . . . . . - 8 -
Installing boards . . . . . - 9 -
Removing boards . . . . . - 10 -

Connectors, Jumper Fields, Factory Defaults . . . . . - 11 -
Connectors . . . . . - 11 -
Jumper Field Factory Defaults . . . . . - 11 -

i960®RP Processor . . . . . - 12 -
General Features . . . . . - 12 -
Additional Documentation . . . . . - 13 -
Clock and Reset Generation . . . . . - 14 -
Clock Generation . . . . . - 14 -
Power-On and Manual Reset . . . . . - 14 -
Hardware Watchdog . . . . . - 15 -
i960®RP Initialization Modes . . . . . - 15 -
Local Memory Devices . . . . . - 17 -
Flash EEPROM . . . . . - 17 -
Dynamic Random Access Memory (DRAM) . . . . . - 18 -
I^2C Interface . . . . . - 19 -
Serial EEPROM 24C32 . . . . . - 19 -
I/O Devices . . . . . - 20 -
CAN Interfaces . . . . . - 20 -
Serial Interface . . . . . - 23 -
Wait States Settings . . . . . - 25 -

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Interrupts . . . . . - 25 -
I/O Interfaces on J2 . . . . . - 26 -
Interrupts . . . . . - 27 -
Diagnostics Display . . . . . - 28 -

CompactPCI ® Interface . . . . . - 29 -
PCI Devices . . . . . - 29 -
Address Translation Unit (ATU) . . . . . - 29 -
System Connector J1 . . . . . - 33 -

Technical Specifications . . . . . - 35 -

Ordering Information . . . . . - 37 -

Figures

Block Diagram . . . . . - 7 -
Installing board into the system rack . . . . . - 9 -
Removing board from the system rack . . . . . - 10 -
Component Assembly Drawing . . . . . - 11 -
Factory Default JCNF . . . . . - 11 -
Clock Selection Jumper JCNF(5) Setting Options . . . . . - 14 -
Jumper Field JCNF . . . . . - 15 -
General I^2C Addressing Byte Format . . . . . - 19 -
Serial EEPROM 24C32 Addressing Byte Format . . . . . - 19 -
Male D-Sub 9 CAN Port Connectors CP1 / CP2 . . . . . - 22 -
RS-232 Port Connector SP1 . . . . . - 24 -

Tables

i960®RP Related Documentation . . . . . - 13 -
Configuration Jumper Field JCNF Initialization Mode Setting Options . . . . . - 15 -
Configuration Jumper Field JCNF BIST Setting Options . . . . . - 16 -
Configuration Jumper Field JCNF CPCI Reset Setting Options . . . . . - 16 -
Flash Device Read And Write Wait State Settings . . . . . - 17 -
DRAM Initialization Parameters . . . . . - 18 -
I/O Device Offset Definitions . . . . . - 20 -
CAN Controller (SJA1000) Register Offset Definitions . . . . . - 20 -
UART Data Transmission Bit-Rates . . . . . - 23 -
UART (16C550) Register Offset Definitions . . . . . - 24 -
Read And Write Wait State Settings . . . . . - 25 -
CompactPCI Connector J2 Pin Assignment . . . . . - 26 -

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Diagnostics Display Information . . . . . - 28 -
Address Translation Unit Configuration Header Format . . . . . - 31 -
ATU Extended PCI Configuration Header Format . . . . . - 31 -
CompactPCI Connector J1 Pin Assignment . . . . . - 33 -
Ordering Information . . . . . - 37 -

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About this Manual

This manual describes the technical aspects of the CX1-BAND, required for installation and system integration. It is intended for the experienced user only.

Edition History

EKF Document	Ed.	Contents/*Changes*	Author	Date
Text # 2443 cx1mle.wpd	1	1. Edition User Manual CX1-BAND English.	gn	2001-03-30
	2	Corrected wrong I/O port offsets. Added info on which port the 82C251 are connected to the SJA1000.	gn	2001-05-21

Nomenclature

Signal names used herein with an attached '#' designate active low lines.

Trade Marks

Some terms used herein are property of their respective owners, e.g.

i960 RP: ® Intel
CompactPCI : ® PICMG
Windows 98, Windows NT, Windows 2000: ® Microsoft

EKF does not claim this list to be complete.

Legal Exclaimer - Liability Exclusion

This manual has been edited as carefully as possible. We apologize for any potential mistake. Information provided herein is designated exclusively to the proficient user (system integrator, engineer). EKF can accept no responsibility for any damage caused by the use of this manual.

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Introduction and Overview

The CX1-BAND is a CompactPCI® based, intelligent fieldbus controller with two independent CAN (Controller Area Network) ports.

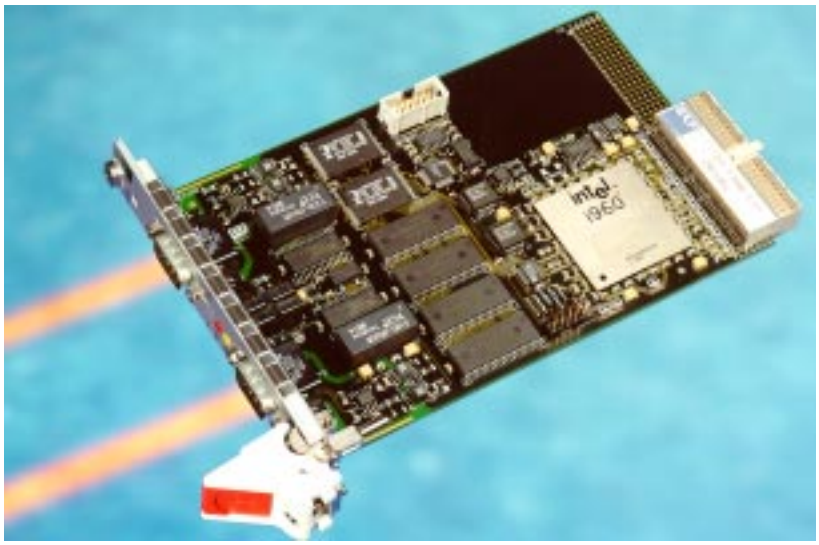
The 3U Eurocard is provided with the i960RP/D (Intel) microprocessor, a powerful 32 bit machine giving freedom for any local data sampling and preprocessing. With its 8MB DRAM and 4MB Flash, the CX1-BAND offers a generous amount of memory.

Two SJA1000 (Philips) act as CAN controllers, incorporating all common protocol levels up to the latest version 2.0B. Both physical transceivers (PCA82C251) are optically isolated between themselves and the remaining circuitry. Each CAN port has its own connector (9-pole D-Sub, wiring according CiA Draft 102).

An additional UART (RS232) can be used as a general communications port, hence simplifying development and testing of on-board firmware, and allowing stand-alone operation of the CX1-BAND.

The CAN connectors CP1 and CP2 protrude through the boards front panel. Two push buttons for reset and NMI are indent mounted in order to prevent from being used inadvertently. A dual LED display reflects the board status.

The serial port SP1 is available from a dual row 2x5 pin PCB receptacle. When using a flat microribbon cable with a 10-pole IDC header on the one end and a 9-pole D-Sub connector on the other, the result is a PC compatible RS232 serial interface port.



CX1-BAND * Dual CAN Controller

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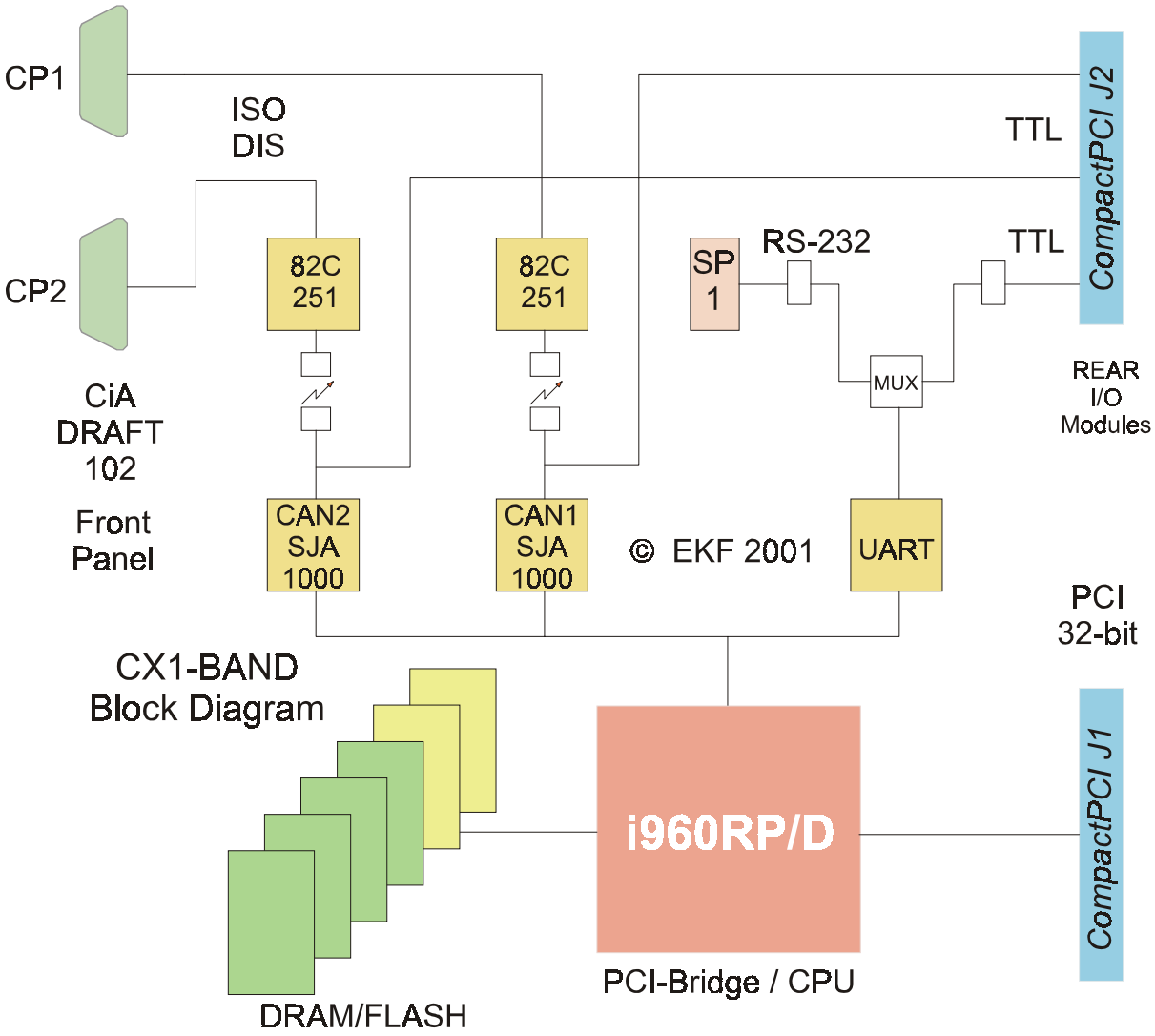
Block Diagram



Block Diagram

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Handling Information

Precautions

This *CompactPCI* ® board contains **electrostatic sensitive** devices. The board should therefore remain in its original EKF packaging until it is used. The antistatic coated film and box provide double protection against electromagnetic discharging as well as against dust, corrosion and mechanical damaging. Be sure to equalize the electrical potential of the board and the *CompactPCI* ® rack before taking out the board of the packaging (by touching the packaging and metallic parts of the rack at the same time, or better by wearing a ground strap). Please keep the original packaging for the case of return. Notice that installing or removing of boards or other system components may done only by authorized persons.

Guidelines to EMC Protection

To fulfill the **CE** specifications with regard to **EMC** take notice of the following guidelines:

- Installation and operation only in EMC systems.
- Close unused system slots with dummy panels.
- Close unused front elements (e.g. RS-232 interfaces) with metallic caps.
- Use shielded cables only.
- Use ferrites to prevent electromagnetic interference (EMI).
- Protect sensible interfaces (e.g. Cheapernet) with plastic caps.

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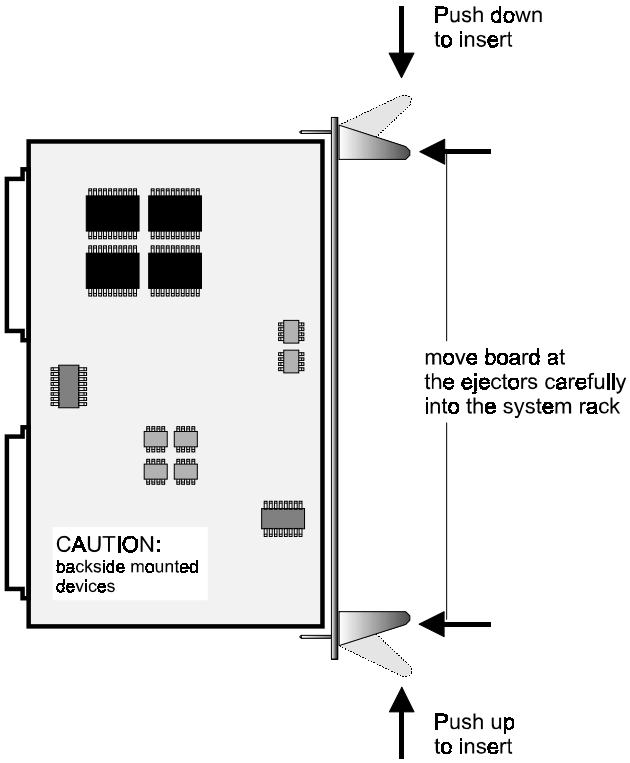
Installing boards

- Switch off the main power supply.
- Touch the system rack to guarantee electrostatic discharge.
- Move board carefully along the guide rails in the chosen slot of the rack. Caution is given especially to the devices mounted on the backside of the circuit board.
- Press the *CompactPCI* ® connectors of the board into the backplane receptacles by pushing the ejectors in the front panel together (see illustration below).
- Optionally screw board and rack together.
- Switch on the main power supply.



Installing board into the system rack

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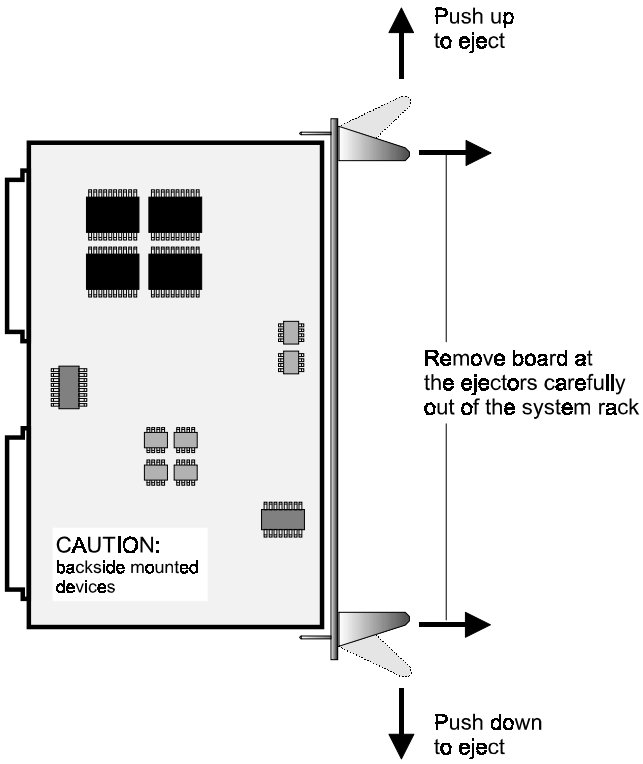
Removing boards

- Switch off the main power supply.
- Touch the system rack to guarantee electrostatic discharge.
- Optionally remove screws if board and rack are mounted together.
- Press the board out of the *CompactPCI* ® backplane by pushing the ejectors in the front panel apart each other (see illustration below).
- Move board carefully along the guide rails out of the rack. Caution is given especially to the devices mounted on the backside of the circuit board.
- Put the removed board in the original EKF packaging box.



Removing board from the system rack

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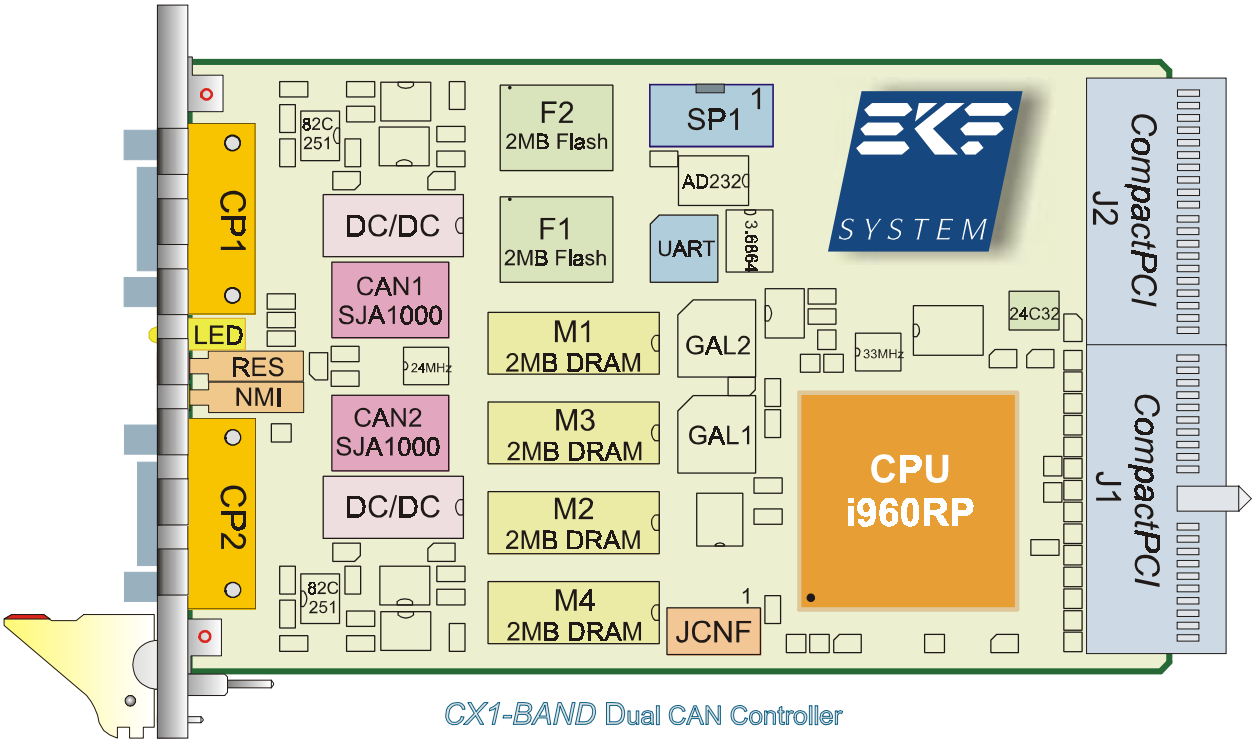
Connectors, Jumper Fields, Factory Defaults

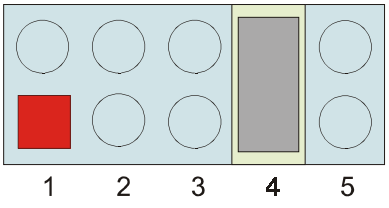


Component Assembly Drawing

Connectors

J1	*CompactPCI* ® Connector
J2	*CompactPCI* ® Connector (CAN Ports 1/2, serial I/O Port, optional)
CP1 / 2	CAN Port 1 and 2 Connectors (9-pin D-Sub)
SP1	RS-232 Serial Interface (10-pin Header)

Jumper Field Factory Defaults



Factory Default JCNF

i960®RP Configuration Selector:

1. Initialization mode 3 (CPU starts after reset)
2. Retry CPCI configuration cycles
3. BIST active
4. CPCI reset passed through to local reset
5. CPCI bus clock in use

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i960®RP Processor

General Features

The central unit on the CX1-BAND is an i960®RP I/O Processor, a member of the 80960 family of high performance processors. It combines a high-speed CPU with powerful features to create an intelligent I/O processor and integrates it into a Peripheral Components Interconnect (PCI) environment. This multi-function PCI device is fully compliant with the *PCI Local Bus Specification*, revision 2.1. The i960®RP local bus, a 32-bit multiplexed burst bus, is a high-speed interface to system memory and I/O. Physical and logical memory attributes are programmed via memory-mapped control registers (MMRs). The core can maintain a sustained execution rate of one instruction per clock of most instructions.

The i960®RP features include:

- Single-clock execution of most instructions
- Independent Multiply/Divide Unit
- 128-bit register bus speeds local register caching
- 4 Kbyte two-way, integrated instruction cache
- 2 Kbyte direct-mapped, integrated data cache
- 1 Kbyte integrated, zero wait state data RAM
- PCI-to-PCI Bridge Unit
- Address Translation Unit
- DMA Controller
- Messaging Unit
- Memory Controller
- I^2C Bus Interface Unit

The Address Translation Unit (ATU) permits direct data access from the ***CompactPCI*** ® interface to local memory. This allows for example the programming of the FLASH devices or downloading software to local memory via the primary *CompactPCI* ® interface without interaction of the i960®RP core. Address translation is controlled through programmable, memory-mapped registers accessible from both the PCI interface and the i960 core processor. The primary ATU has a dedicated PCI configuration space that is accessible through the *CompactPCI* ® bus or the i960 core.

The DMA Controller allows low-latency, high-throughput data transfers between PCI bus agents and i960®RP local memory. Three separate DMA channels accommodate data transfers: two for the *CompactPCI* ® bus, one for the secondary PCI bus (not usable on the CX1-BAND). The DMA Controller supports chaining and unaligned data transfers.

The Messaging Unit (MU) provides data transfer between the PCI system and the i960®RP. It uses interrupts to notify each system when new data arrives. The MU has four messaging mechanisms: Message Registers, Doorbell Registers, Circular Queues and Index Registers. Each allows a host processor or external PCI device and the i960®RP to communicate through message passing and interrupt generation. The MU makes it easy to realize the Intelligent I/O Interface I_2O.

The Memory Controller allows direct control of the external memory on the CX1-BAND, including DRAM and Flash EEPROM. It features programmable chip selects and a wait state

generator. External memory can be configured as PCI addressable memory or private i960®RP memory.

Since there is no need for it, the secondary PCI interface of the i960®RP is unconnected on the CX1-BAND. Therefore it whether makes sense to use the PCI-to-PCI Bridge unit nor the secondary ATU.

Additional Documentation

A detailed description of these and other features including the programming of the i960®RP processor could be find in the documentation listed below. Electronic information can be obtained via

http://www.intel.com

i960®RP Related Documentation

Document Title	Order Number
i960®Rx I/O Microprocessor Developer's Manual	Intel Order # 272736
i960®Rx I/O Processor Specification Update	Intel Order # 272918
i960®RP/RD I/O Processor at 3.3 Volts data sheet	Intel Order # 273001
i960®Jx Microprocessor User's Guide	Intel Order # 272483

Clock and Reset Generation

Clock Generation

The CX1-BAND is clocked by a single, 33 MHz signal. This master clock controls the entire timing of the i960®RP. The main clock input is fed by one of two possible sources, chosen by jumper 5 of the 5x2 configuration jumper **JCNF** near the CPU on the CX1-BAND:

Clock Selection Jumper JCNF(5) Setting Options

Clock Source	JCNF(5)
CompactPCI ® Bus Clock Signal (**J1** Pin D6)	removed
33 MHz Oscillator on the CX1-BAND	set

Normally the CX1-BAND will be integrated in a *CompactPCI* ® rack with a system controller and possibly other boards. In this case always the bus clock signal should be used as clock source (**JCNF(5)** removed!).

To support a single stand-alone operation without system controller the CX1-BAND provides an on-board 33 MHz oscillator that generates the necessary clock. When setting the jumper **JCFN(5)** the oscillators output is connected to the clock input of the board.

CAUTION:
Note that in this case the clock signal also occurs on the clock pin of the *CompactPCI* ® connector **J1** (Pin D6). This will lead to clock signal crashing on the bus if more than one board drives the clock.

The clock signal is distributed on the CX1-BAND via a dedicated clock buffer to provide a low skew, well conditioned signal as required by the PCI specification.

Power-On and Manual Reset

There are a lot of reasons which trigger a reset on the CX1-BAND:

(1) Power-On (switching on the power supply)
(2) V_{cc5} drops below 4.65V (power failed)
(3) V_{cc3} drops below 3.0V (power failed)
(4) Pushing the **RESET** Push Button in the front panel
(5) Triggering the *CompactPCI* ® reset signal (**J1** Pin C5, **JCNF**(4) on)
(6) Reaching time out of the hardware watchdog
(7) Software reset caused by the i960®RP processor

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The first 6 sources will reset all devices on the CX1-BAND to a known state. An integrated power supervisor generates a clean reset signal with a minimum length of 140 ms even if the voltages haven't stabilized at power-on. The signal is fed to the i960®RP, the Flash EEPROMs, the two CAN controllers SJA1000 and the serial controller 16C550. The processor can reset all the SJA1000s and the 16C550 by triggering the local bus reset signal in the Extended Bridge Control Register (EBCR, bit 5).

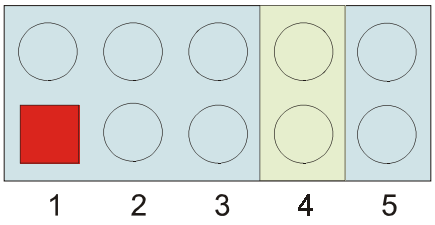
Hardware Watchdog

The CX1-BAND is equipped with a hardware watchdog. The watchdog is disabled after a hardware reset. It is activated by toggling the general purpose output OUT1# of the 16C550. This is done by changing bit 2 in the Modem Control Register MCR of the UART (see section *Serial Controller 16C550* for details of the UART's registers).

If the processor once touched MCR(2), the watchdog is armed and must be triggered at least every 1000 ms. A hardware reset will occur after a maximum time of 1.6 sec after the last watchdog trigger pulse.

i960®RP Initialization Modes

The behavior of the i960®RP after reset is controlled by the configuration selection jumper field JCNF. The processor supports four initialization modes 0 to 3, where mode 1 makes no sense on the CX1-BAND.



Jumper Field JCNF

Configuration Jumper Field JCNF Initialization Mode Setting Options

Initialization Mode	JCNF(1)	JCNF(2)	*CompactPCI* ® Interface	i960RP core processor
Mode 0	set	set	accepts transactions	held in reset
Mode 1 [1])	set	removed	retries all config. transactions	held in reset
Mode 2	removed	set	accepts transactions	initializes
Mode 3	removed	removed	retries all config. transactions	initializes

[1]) Not useful on the CX1-BAND

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Mode 0 allows a host processor to configure the i960®RP peripherals while the i960 core processor is held in reset. The host processor configures the PCI-to-PCI bridge by assigning bus numbers, allocating PCI address space, and assigning IRQ numbers. The memory controller and ATU can also be initialized by the host processor. Program code for the i960 core processor may be downloaded into local DRAM or Flash EEPROM by the host processor. The host processor then clears the i960 reset signal by clearing the Core Processor Reset bit in the Extended Bridge Control Register (EBCR, bit 1). This deasserts the internal reset signal on the i960 core processor and the processor begins its initialization process.

Mode 2 allows configuration cycles on the PCI-to-PCI bridge at any time and allows the i960 core processor to initialize after reset. Mode 2 allows each unit of the i960®RP to be initialized in its own manner. Be aware that race conditions may exist between i960 core operation after reset and host processor PCI configuration.

Mode 3 allows the i960 core processor to initialize and control the initialization process before the host processor is allowed to configure the i960®RP peripherals. During this time, the *CompactPCI* ® interface signals a Retry on all configuration cycles it receives until the i960 core processor clears the Configuration Cycle Disable bit in the EBCR.

The 3rd jumper of JCNF exists to enable or disable the i960®RP's build-in self test (BIST). If enabled the processor tries to check all its internal units. If the check failed the processor asserts a signal that lights the red on-board LED CPU FAIL and core execution stops. Because BIST needs about 414000 CPU cycles it may be necessary to disable it when the restart time needs to be minimized.

Configuration Jumper Field JCNF BIST Setting Options

JCNF 3	Processor BIST
removed	enabled
set	disabled

Jumper 4 of JCNF is used to forward the reset signal from the *CompactPCI* ® bus to the CPU and the other local devices on the board.

Configuration Jumper Field JCNF CPCI Reset Setting Options

JCNF 4	CPCI Reset
removed	ignored
set	forwarded to the board

It is a good idea to remove JCNF 4 when the BIOS of the main CPU board within the *CompactPCI* ® does not recognize the CX1-BAND after system reset.

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Local Memory Devices

Flash EEPROM

The CX1-BAND is equipped with on-board programmable Flash EEPROM devices. The data bus width to these devices is 32-bit allowing the i960®RP to execute program code from Flash in full speed. Therefore it is not necessary to copy the code into DRAM. The Flash devices are connected to the memory bank 0 of the i960®RP Memory Controller. They are readable and especially writeable any time with no need to enable the programming voltage. Caution is given when the processor itself tries to program the Flash devices while executing code from the Flashs. This will lead to a hanging processor core. To program the Flash devices use one of the following alternates:

1. Programming by i960®RP core processor: Copy the program data and the Flash programming algorithm code to DRAM. Run the programming code from DRAM. Return to the calling function or restart the code loaded into the Flash devices.

2. Programming via *CompactPCI* ® interface: Reset the CX1-BAND with JCNF setting to initialization mode 0. Alternatively the i960®RP core processor could be halted by executing the HALT instruction. Program the Flash devices via the primary ATU. Restart the processor.

Depending on the version of the CX1-BAND there are different types of Flash devices in use:

- 28F016SV / Intel
- 28F160S5 / Intel

These devices distinguish in access times and programming algorithms. Programming tools (currently running on LINUX or WinXX) are offered by EKF and are available on request. The following table shows the necessary initializations in the read and write wait state registers (MBRWS0, MBWWS0) of the i960®RP memory controller dependent on the devices in use. All timing parameters are based on a clock frequency of 33.33 MHz (corresponding to 30 ns cycle time):

Flash Device Read And Write Wait State Settings

Flash Device	Read		Write	
	Access [ns]	MBRWS0	Access [ns]	MBWWS0
28F016SV	70	0x00000220	70	0x00000221
28F160S5	70	0x00000220	70	0x00000220

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Dynamic Random Access Memory (DRAM)

The CX1-BAND offers a working memory space of 8 Mbyte. The memory is organized in two banks of non-interleaved DRAM, each 4 Mbyte in size. The data path width is 32-bit without parity. Similar to the Flash EEPROMs different types of DRAM devices are in use. Possible types are

- Fast Page Mode (FPM) DRAMs
- Extended Data Out (EDO) DRAMs

with an access time of at least 70 ns. The following table shows typical values to program to the i960®RP memory controller to setup the DRAM interface. All timing parameters are based on a clock frequency of 33.33 MHz (corresponding to 30 ns cycle time):

DRAM Initialization Parameters

Name	Register	Value	Description
DRWS	DRAM Bank Read Wait State	0x00000000	RAS-to-CAS delay 1.5 cycles, CAS pulse width 1.5 cycles, no additional recovery wait states
DWWS	DRAM Bank Write Wait State	0x00000000	RAS-to-CAS delay 1.5 cycles, CAS pulse width 1.5 cycles, no additional recovery wait states
DRIR	DRAM Refresh Interval	0x00010204	Refresh enabled, 15.625 µs refresh interval
DPER	DRAM Parity Enable	0x00000000	DRAM parity disabled
DBCR	DRAM Bank Control	0x0000000D 0x0000004D	High-current drives disabled, DRAM bank enables, Fast Page Mode (FPM), 2 banks or Extended Data Out (EDO), 2 banks

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I²C Interface

The i960®RP supports a master and slave interface to the popular I²C (Inter-Integrated Circuit) bus. This simple, two wire serial bus allows an easy connection to other I²C devices. Transfer rates of up to 400 Kbit/s are possible. It could be programmed via the I²C unit registers of the i960®RP.

An I²C message consists of a device addressing byte and additional data bytes. The device address byte also contains the information whether the following operations are read or write transfers. If the address of an I²C slave device on the bus matches the device address byte sent by a master, the slave acknowledges the transfer.

General I²C Addressing Byte Format

A_6	A_5	A_4	A_3	A_2	A_1	A_0	R/W
MSB							LSB

On write operations (R/W=0) the master may send then further data bytes to the slave until the master generates a stop condition. Each byte transferred is acknowledged by the recipient. Read operations are working in the same way except that R/W=1 and that the data flow is reversed.

Serial EEPROM 24C32

The CX1-BAND offers a serial EEPROM 24C32 with a capacity of 4 Kbytes. This device can be used e.g. to permanently store important parameters that should be non volatile even if the power disappears. It is accessible as slave device via the I²C bus. Write accesses to the memory array of the serial EEPROM are possible any time because the hardware write protection feature of the 24C32 is not enabled on CX1-BAND.

Serial EEPROM 24C32 Addressing Byte Format

1	0	1	0	0	0	0	R/W
MSB				A_2	A_1	A_0	LSB

The above figure shows the I²C bus device addressing byte that must be written to the serial EEPROM in order to read (R/W=1: DeviceAddr=0xA1) or write (R/W=0: DeviceAddr=0xA0) data from or to it (the 3 external address lines A_{2-0} offered by the 24C32 are hard-wired to GND on the CX1-BAND). Read and write accesses with the I²C bus maximum speed of 400 Kbit/s are supported by the device.

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I/O Devices

The CX1-BAND contains two CAN2.0B compatible interfaces and one serial RS-232 interface. These I/O devices are connected to bank 1 of the i960®RP's memory controller. The following table shows the addressing of the devices relative to the base address of memory bank 1:

I/O Device Offset Definitions

Device	UART	CAN Port 1	CAN Port 2
Base Address Offset	0x0000	0x2000	0x3000

CAN Interfaces

The two CAN2.0B compatible interfaces on the CX1-BAND are realized with a SJA1000 (Philips) CAN controller and a 82C251 CAN bus transceiver for each port. Therefore the board is designed to connect to standard 24 V systems (according the "ISO 11898 - 24 V" standard) with transfer rates up to 1 MBaud. Both ports are opto-isolated against the *CompactPCI* backplane and also against each other. The bus transceivers connect to the CAN controller via port 0 (TX0/RX0) of the SJA1000.

The CAN controllers are connected to bank 1 of the i960®RP's memory controller. See table *I/O Device Offset Definitions* above for the address of the CAN port controllers within the i960®RP's memory map. The following table shows the addressing of the registers of the SJA1000 relative to its base address:

CAN Controller (SJA1000) Register Offset Definitions [1])

Base Address Offset	Read Access	Write Access
0x00	control	control
0x01	0xFF	command
0x02	status	not allowed
0x03	interrupt	not allowed
0x04	acceptance code [2])	acceptance code [2])
0x05	acceptance mask [2])	acceptance mask [2])
0x06	bus timing 0 [2])	bus timing 0 [2])
0x07	bus timing 1 [2])	bus timing 1 [2])
0x08	output control [2])	output control [2])

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Base Address Offset	Read Access	Write Access
0x09	test	test
0x0A	Transmit ID 10-3	Transmit ID 10-3
0x0B	Transmit ID 2-0, RTR and DLC	Transmit ID 2-0, RTR and DLC
0x0C	Transmit Data Byte 1	Transmit Data Byte 1
0x0D	Transmit Data Byte 2	Transmit Data Byte 2
0x0E	Transmit Data Byte 3	Transmit Data Byte 3
0x0F	Transmit Data Byte 4	Transmit Data Byte 4
0x10	Transmit Data Byte 5	Transmit Data Byte 5
0x11	Transmit Data Byte 6	Transmit Data Byte 6
0x12	Transmit Data Byte 7	Transmit Data Byte 7
0x13	Transmit Data Byte 8	Transmit Data Byte 8
0x14	Receive ID 10-3	Receive ID 10-3
0x15	Receive ID 2-0, RTR and DLC	Receive ID 2-0, RTR and DLC
0x16	Receive Data Byte 1	Receive Data Byte 1
0x17	Receive Data Byte 2	Receive Data Byte 2
0x18	Receive Data Byte 3	Receive Data Byte 3
0x19	Receive Data Byte 4	Receive Data Byte 4
0x1A	Receive Data Byte 5	Receive Data Byte 5
0x1B	Receive Data Byte 6	Receive Data Byte 6
0x1C	Receive Data Byte 7	Receive Data Byte 7
0x1D	Receive Data Byte 8	Receive Data Byte 8
0x1E	0xFF	not allowed
0x1F	clock divider	clock divider [3])

Notes:
[1]) Register set is shown in BasicCAN mode.
[2]) Only valid for reset mode.
[3]) Some bits are writeable in reset mode only.

A detailed description of the SJA1000 operation is given in the "*SJA1000 Stand-alone CAN controller*" data sheet delivered by Philips Semiconductors.

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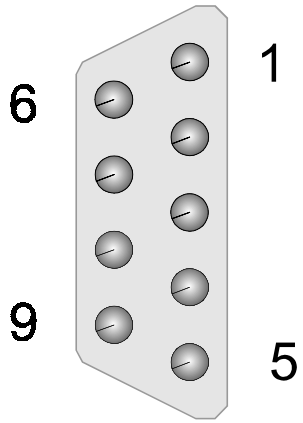
The signals of the CAN ports are fed to the two 9-pin D-Sub connectors **CP1** and **CP2** in the front panel of the board. The illustration below shows the pin assignments of the connectors **CP1 / CP2** (front view of the connectors), which was chosen according the CiA Draft 102.



Male D-Sub 9 CAN Port Connectors CP1 / CP2

CP1 / CP2		
	1	
CAN GND	6	
	2	CAN LOW
CAN HIGH	7	
	3	CAN GND
	8	
	4	
	9	
	5	SHIELD

The CX1-BAND offers the possibility to be used in a *CompactPCI* rear I/O environment. The receive and transmit signals provided by the SJA1000 are fed to the optional equipped *CompactPCI* connector **J2** for each CAN port (see also the block diagram of the CX1-BAND). That allows the use of a customer specific transition module on the back side of a *CompactPCI* rack. In this configuration the transition module should also include the CAN bus transceivers. Ask EKF for such a solution.

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Serial Interface

For service or debugging the CX1-BAND provides a serial RS-232 interface. The signals of this port are fed to the 10-pin header **SP1** and to the optional equipped *CompactPCI* connector **J2** (TTL signals only). Adapters to change to a common used 9-pin D-Sub connector are available by EKF. This allows to make simple links to serial interfaces of terminals, personal computers, modems etc. with usual cables.

The serial interface is based on the well known Asynchronous Communication Element (ACE) 16C550. This UART is clocked with a separate 14.7456 MHz oscillator leading to transfer rates of up to 921.6 kBaud. Due to the fact that the 16C550 could be clocked up to 16 MHz, higher baud rates are also possible by using an accordingly oscillator (deliverable on request).

The next table shows the transmission bit rates, the value of the UART's divisor latch register (iDiv) and the resulting baud rate errors in dependency of the clock in use:

UART Data Transmission Bit-Rates

Clock	Baud	Divisor	iDiv	Error
14745600	75	12288.0	12288	0.00%
14745600	110	8378.2	8378	0.00%
14745600	150	6144.0	6144	0.00%
14745600	300	3072.0	3072	0.00%
14745600	600	15360	1536	0.00%
14745600	1200	768.0	768	0.00%
14745600	1800	512.0	512	0.00%
14745600	2400	384.0	384	0.00%
14745600	4800	192.0	192	0.00%
14745600	7200	128.0	128	0.00%
14745600	9600	960	96	0.00%
14745600	14400	64.0	64	0.00%
14745600	19200	48.0	48	0.00%
14745600	38400	24.0	24	0.00%
14745600	56000	16.5	16	-2.78%
14745600	57600	16.0	16	0.00%
14745600	115200	8.0	8	0.00%
14745600	128000	7.2	7	-2.78%
14745600	230400	4	4	0.00%

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Clock	Baud	Divisor	iDiv	Error
14745600	460800	2	2	0.00%
14745600	921600	1	1	0.00%

The UART is connected to bank 1 of the i960®RP's memory controller. See table *I/O Device Offset Definitions* above for the address of the serial port controller within the i960®RP's memory map. The following table shows the addressing of the registers of the UART relative to its base address:

UART (16C550) Register Offset Definitions

Base Address Offset	Read Access	Write Access
0x00	Receiver Buffer Register (**RBR**)	Transmitter Holding Register (**THR**)
0x04	Interrupt Enable Register (**IER**)	Interrupt Enable Register (**IER**)
0x08	Interrupt Ident. Register (**IIR**)	FIFO Control Register (**FCR**)
0x0C	Line Control Register (**LCR**)	Line Control Register (**LCR**)
0x10	Modem Control Register (**MCR**)	Modem Control Register (**MCR**)
0x14	Line Status Register (**LSR**)	not allowed
0x18	Modem Status Register (**MSR**)	ignored
0x1C	Scratch Register (**SCR**)	Scratch Register (**SCR**)

The next figure shows the pin assignment of the 10-pin header SP1 providing the serial RS-232 port.

RS-232 Port Connector SP1

SP1			
	1	2	
RXD#	3	4	RTS
TXD#	5	6	CTS [1])
RTS	7	8	
GND	9	10	

Note: [1]) This signal is pulled up by a 2.4kΩ resistor to +5V.

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Wait States Settings

In order to get a proper function of the CAN controllers and the UART, the following values should be programmed to the wait state registers of memory bank 1. Burst accesses to these devices are **not** allowed.

I/O Devices Read And Write Wait State Settings

MBRWS1	MBWWS1
0x00000302	0x00000302

Interrupts

Both the CAN controllers and the UART are able to request i960®RP core interrupts. On the CX1-BAND all these devices share the common interrupt request XINT0#.

An IRQ can be identified by checking the interrupt status register of either the CAN controllers or the UART in the interrupt service routine. The request is released by accessing the corresponding register of the device that caused the interrupt (e.g. reading the interrupt status register of a CAN controller or reading an incoming character from the RBR of the UART). See the data sheets of the SJA1000, the 16C550 and the i960®RP manual for detailed description of interrupt programming.

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I/O Interfaces on J2

To allow a maximum flexibility the CX1-BAND offers an interface to external transition modules via the *CompactPCI* ® connector **J2**. The signals of both CAN ports as well as the serial interface (TTL signals) are connected to **J2**.

CompactPCI Connector J2 Pin Assignment

#J2	A	B	C	D	E
22	NC	NC	NC	NC	NC
21	NC	NC	NC	NC	NC
20	NC	NC	NC	NC	NC
19	NC	NC	NC	NC	NC
18	NC	NC	NC	NC	NC
17	NC	NC	NC	NC	NC
16	NC	NC	NC	NC	NC
15	NC	NC	NC	NC	NC
14	NC	NC	NC	NC	NC
13	NC	NC	NC	NC	NC
12	NC	NC	NC	NC	NC
11	NC	NC	NC	NC	NC
10	NC	NC	NC	NC	NC
9	NC	NC	NC	NC	NC
8	GND	NC	NC	CANRX2	NC
7	NC	NC	CANTX2	NC	+5V
6	GND	NC	NC	CANRX1	NC
5	NC	NC	CANTX1	NC	+5V
4	NC	NC	NC	NC	NC
3	NC	NC	NC	NC	NC
2	GND	CTS#	NC	RXD	NC
1	NC	RTS#	TXD	NC	+5V
#J2	**A**	**B**	**C**	**D**	**E**

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Interrupts

The i960®RP provides an on-chip programmable interrupt controller that allows a flexible, priority level based reaction to internal and external events. The processor uses interrupt vector numbers to enter the interrupt service routine (ISR). This mechanism leads to fast reaction and low interrupt latency. To optimize interrupt performance the vectors can be hold in the i960®RP internal RAM and the ISR can be frozen in the instruction cache. See the i960®RP manual for details.

Internal interrupt events have their origin by the different units within the i960®RP like the I^2C unit, the messaging unit etc. External requests are fed to the processor via 8 maskable (XINT0#...XINT7#) and one non-maskable (NMI#) interrupt inputs. Four bits within the PCI interrupt routing select register (PIRSR) decide for each XINT#-pin whether the interrupt is lead to the i960 core or to the *CompactPCI* ® interface.

The CX1-BAND owns the following peripheral interrupt devices:

(1) the CAN controllers SJA1000 and the UART via XINT0#
(2) the NMI push button via NMI# (non-maskable!)

For a description of the CAN controller respective the serial controller interrupts refer to the corresponding section of this manual.

The NMI push button is a nice tool when debugging software on the CX1-BAND. A debugger can enter the control of a running program when pushing the NMI push button. Because this interrupt can not be masked by a program, getting program control is always possible. The interrupt request of the NMI button is active while the button is pushed. It can be identified by checking the NMI interrupt status register (NISR, bit 8).

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Diagnostics Display

There are two LEDs on the CX1-BAND indicating the current state of the board. These LEDs are mounted in the front panel and having to following meaning:

Diagnostics Display Information

LED	lighten	not lighten
ERR	build-in self test failed, or local bus confidence test failed, or processor held in reset state: core execution stopped	both build-in self test and local bus confidence test passed: core is in executing mode
LOC	access to local DRAM, Flash, CAN Controllers or UART	no access to any local device

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CompactPCI ® Interface

The CX1-BAND offers a *CompactPCI* ® interface complying to the *CompactPCI* ® *Specification Revision 2.1*. *CompactPCI* ® is an industrial implementation of the familiar *Peripheral Component Interconnect* (PCI) bus. It combines the well known electrical features of PCI with the more robust mechanical 19 inch rack mounting technology. The interface supports 64-bit address and 32-bit data transfers. It is designed for a clock frequency of 33 MHz with a transfer rate of up to 132 Mbyte/s.

PCI Devices

The *CompactPCI* ® interface is realized by the i960® RP processor. It consists of two PCI functions, thus it is a multi-function PCI device. The first function (PCI function 0) is the PCI-to-PCI bridge unit which creates a data path between the primary (the *CompactPCI* ®) and the secondary interface (not used on CX1-BAND). PCI function 1 is the primary Address Translation Unit (ATU). This unit allows high-speed accesses from the *CompactPCI* ® interface to the local bus devices like Flash EEPROM or DRAM. Normally a BIOS running on a host system detects these PCI devices at boot time.

Address Translation Unit (ATU)

The Address Translation Unit (ATU) provides an interface between the *CompactPCI* ® bus and the i960 local bus. It consists of two parts: the primary ATU for accesses from *CompactPCI* ® and the secondary ATU for accesses from the secondary PCI bus (not used on the CX1-BAND). Data transfers initiated by any PCI bus master to a local bus device are called *inbound* transactions. If the i960 core starts a data access to any PCI bus slave, this is called an *outbound* transfer.

The ATU fulfils both address filtering and address translation. For inbound transactions the ATU uses three registers:

- Inbound ATU Base Register
- Inbound ATU Limit Register
- Inbound ATU Translate Value Register

A PCI address is detected as an inbound transaction by the ATU if

(PCI_Address & Limit_Register) == Base_Register.

The incoming 32-bit PCI_Address is bitwise ANDed with the Limit_Register. When the result matches the Base_Register, the PCI_Address is detected as being within the inbound translation window. This opens a PCI address window from (Base_Register) to (Base_Register + Limit_Register). Once the transaction is claimed, the address must be

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translated from a 32-bit PCI address to a 32-bit local address. For that the incoming PCI_Address is first bitwise ANDed with the bitwise inverse of the Limit_Register. This result is bitwise ORed with the ATU Translate_Value_Register. The result is the 32-bit local address:

Local_Address = (PCI_Address & (~Limit_Register)) | Translate_Value_Register

In addition the ATU provides address detection and translation for i960 core processor-initiated cycles targeted to one of the PCI buses. The ATU supports two different translation modes:

- Address Translation Windows
- Direct Addressing Window

The address translation windows are located from 0x8000 0000 to 0x9001 FFFF within the 32-bit local address space of i960 processor. This range consists of two 128 Mbyte memory windows and two 64 Kbyte I/O windows for the primary and secondary ATU respectively. Each memory window is divided into two areas, 64 Mbyte for 32-bit PCI address cycles and 64 Mbyte for PCI double address cycles (DAC). The type of the PCI transfer is dependent from the area that is hit within the address translation window by the i960 core.

The translation mechanism used is very similar to the algorithm for the inbound transactions descript above. For memory and DAC accesses it is

PCI_Address = (Local_Address & 0x03FF FFFF) | Memory_Window_Value_Register

I/O transactions are translated by

PCI_Address = (Local_Address & 0x0000 FFFF) | I/O_Window_Value_Register

In addition the i960®RP provides a direct addressing scheme. This methode of outbound PCI transactions is limited to memory transfers and works within the local address range from 0x0000 2000 to 0x7FFF FFFF only. If enabled any access to these locations are forwarded to the PCI bus. Which of the PCI buses are used will be decided by a bit in the ATU control register ATUCR. This register also contains the direct addressing enable bit.

As every PCI device the ATU implements its own configuration space. This space is 256 bytes in size, whereas the first 64 bytes must adhere to a predefined header format. The ATU is programmed on the *CompactPCI* ® interface via type 0 configuration commands to PCI function number one. Besides the i960 core processor can access the configuration space via memory mapped registers at local address 0x1200. Some of the read-only registers can also be written by the i960. The following table shows the configuration header according the *PCI Local Bus Specification*, revision 2.1:

Address Translation Unit Configuration Header Format

Address Translation Unit Configuration Header				Address Offset
ATU Device ID		ATU Vendor ID		0x00
ATU Primary Status		ATU Primary Command		0x04
ATU Class Code			ATU Revision ID	0x08
BIST	Header Type	Latency Timer	Cacheline Size	0x0C
Primary Inbound ATU Base Address				0x10
Reserved				0x14
				0x18
				0x1C
				0x20
				0x24
				0x28
ATU Subsystem ID		ATU Subsystem Vendor ID		0x2C
Expansion ROM Base Address				0x30
Reserved				0x34
				0x38
Max. Latency	Minimum Grant	Interrupt Pin	Interrupt Line	0x3C

The next table shows the i960®RP specific registers of the ATU configuration space.

ATU Extended PCI Configuration Header Format

ATU Extended PCI Configuration Register Space	Address Offset
Primary Inbound ATU Limit Register PIALR	0x40
Primary Inbound ATU Translate Value Register PIATVR	0x44
Secondary Inbound ATU Base Address Register SIABAR	0x48
Secondary Inbound ATU Limit Register SIALR	0x4C
Secondary Inbound ATU Translate Value Register SIATVR	0x50
Primary Outbound Memory Window Value Register POMWVR	0x54
Reserved	0x58
Primary Outbound I/O Window Value Register POIOWVR	0x5C
Primary Outbound DAC Window Value Register PODWVR	0x60

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ATU Extended PCI Configuration Register Space		Address Offset
Primary Outbound Upper 64-bit DAC Register POUDR		0x64
Secondary Outbound Memory Window Value Register SOMWVR		0x68
Secondary Outbound I/O Window Value Register SOIOWVR		0x6C
Reserved		0x70
Expansion ROM Base Address Register ERBAR		0x74
Expansion ROM Translate Value Register ERTVR		0x78
Reserved		0x7C
		0x80
		0x84
ATU Configuration Register ATUCR		0x88
Reserved		0x8C
Primary ATU Interrupt Status Register PATUISR		0x90
Secondary ATU Interrupt Status Register SATUISR		0x94
Secondary ATU Status Register	Secondary ATU Commond Register	0x98
Secondary Outbound DAC Window Value Register SODWVR		0x9C
Secondary Outbound Upper 64-bit DAC Register SOUDR		0xA0
Primary Outbound Configuration Cycle Address Register POCCAR		0xA4
Secondary Outbound Configuration Cycle Address Register SOCCAR		0xA8
Primary Outbound Configuration Cycle Data Register POCCDR		0xAC
Secondary Outbound Configuration Cycle Data Register SOCDCR		0xB0
Reserved		0xB4 - 0xFF

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System Connector J1

The *CompactPCI* ® specification defines the usage of shielded, 2 mm-pitch, 5-row connectors on *CompactPCI* ® boards according to IEC 917 and IEC 1076-4-101. The 32-bit PCI interface is implemented via the **J1** connector, while the 64-bit option requires the connector **J2**. Since the CX1-BAND has a 32-bit *CompactPCI* ® interface the **J2** connector is not necessary. Alternatively the **J2** connector can be used to realize rear I/O. Since this requires a special *CompactPCI* back plane, **J2** is mounted only when rear I/O is requested.

The **J1** connector also defines the supported signaling voltage ($V_{I/O}$). A coding key in this connector is used to distinguish boards with $V_{I/O}$ = 3.3 V (cadmium yellow key), $V_{I/O}$ = 5 V (brilliant blue key) or both (no key). The CX1-BAND is laid out for $V_{I/O}$ = 5 V only and equipped with a blue coding key.

CAUTION:

Do not use the CX1-BAND within a 3.3 V *CompactPCI* ® system.

CompactPCI Connector J1 Pin Assignment

#J1	A	B	C	D	E
25	5V	REQ64# [1])	ENUM# [1])	3.3V	5V
24	AD1	5V	VI/O	AD0	ACK64# [1])
23	3.3V	AD4	AD3	5V	AD2
22	AD7	GND	3.3V	AD6	AD5
21	3.3V	AD9	AD8	M66EN [2])	C/BE0#
20	AD12	GND	VI/O	AD11	AD10
19	3.3V	AD15	AD14	GND	AD13
18	SERR#	GND	3.3V	PAR	C/BE1#
17	3.3V	SDONE [1])	SBO# [1])	GND	PERR#
16	DEVSEL#	GND	VI/O	STOP#	LOCK#
15	3.3V	FRAME#	IRDY#	GND	TRDY#
14	Coding Key Area (Brilliant Blue)				
13					
12					
11	AD18	AD17	AD16	GND	C/BE2#
10	AD21	GND	3.3V	AD20	AD19

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9	C/BE3#	IDSEL	AD23	GND	AD22
8	AD26	GND	VI/O	AD25	AD24
7	AD30	AD29	AD28	GND	AD27
6	REQ#	GND	3.3V	CLK	AD31
5	BRSVP1A5 [1])	BRSVP1B5 [1])	RST#	GND	GNT#
4	BRSVP1A4 [1])	GND	VI/O	INTP [1])	INTS [1])
3	INTA#	INTB#	INTC#	5V	INTD#
2	TCK	5V	TMS	TDO	TDI
1	5V	-12V	TRST#	+12V	5V
#J1	**A**	**B**	**C**	**D**	**E**

Notes:
[1]) These pin positions are not connected on the CX1-BAND.
[2]) This signal is hardwired to GND on the CX1-BAND.

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Technical Specifications

System-Processor i960®RP and local Devices

- CPU Core
  - Based on the i960JF high performance core
  - Highest throughput at low power consumption (33 MHz/3.3 V)
  - Integrated 4 KB instruction and 2 KB data cache
  - 1 KB internal data RAM

- Memory
  - 8 MB FPM or EDO DRAM
  - 4 MB Flash ROM (32-Bit), on-board programmable
  - Up to 4 KB burst transfers
  - 32 Kbit serial EEPROM

- I/O
  - Two CAN2.0B interfaces on male D-Sub 9 front panel connectors **CP1**, **CP2** (max. 1 MBit/s), connected also to *CompactPCI* ® **J2** connector
  - RS-232 serial interface on 10-pin header (max. 230 kBit/s), connected also to *CompactPCI* ® **J2** connector (TTL signals)

- Diagnostics/Debugging
  - LED ERR: i960RP initializing fault
  - LED LOC: access to local peripherals or memory
  - Reset push button switch
  - NMI push button switch (software abort function)

CompactPCI ® Bus

- 3 U height, 20.32 mm width
- 32-Bit PCI interface 33 MHz (max. data transfer rate 132 MB/s)
- PCI 64-Bit dual address cycles
- Up to 64 byte PCI bursts
- $V_{I/O}$=5V
- Complies to *CompactPCI* ® *Specification*, revision 2.1

EKF Elektronik GmbH * Philipp-Reis-Str. 4 * D-59065 HAMM (Germany)
Tel. +49 (0)2381/6890-0 * Fax. +49 (0)2381/6890-90 * E-Mail info@ekf.de * Internet http://www.ekf.de

Power Consumption

- +5 V ± 5% : 1.0 A max.
- +3.3 V ± 0.3V : 1.1 A max.
- +12 V ± 5% : 0 mA max.
- -12 V ±5 % : 0 mA max.

Temperature, Humidity

- Operating temperature 0-70˚ C
- Humidity 5-90%, non condensing

Technical specifications are subject to change

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Ordering Information

Ordering Information

Short Alias	Ordering No.	Description
BAND	CX1-1-BAND	3U, intelligent dual CAN 2.0B host adapter, 2 x CAN controller SJA1000, optically isolated, CPU i960RP, 33MHz, 8MB DRAM, 4MB Flash ROM, RS-232, *CompactPCI* Interface 32-Bit/132 Mbit/s
	CR9-1-ADAPT	Front panel expansion adapter for 3U board mounting in 6U racks, suitable for all EKF 3U (4HP) boards, mounting kit includes all required parts

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